**Cell Description:**This is a standard single-bit, positive-edge triggered flip-flop with an asynchronous, active low clear signal. The input signal to this cell is sampled on the rising edge of the clock signal, only the sampled signal is available at the output of the cell.

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **CLK** | **D** | **CLRBAR** | **Q** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | Q |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | Q |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "DFF" "behavioral"

module DFFQ( Q, CLRB, CLK, D );

input CLRB;

input CLK;

input D;

output reg Q;

always@(posedge CLK or negedge CLRB) // Async clear

begin

if(~CLRB) //Active low clear

Q <= 1'b0;

else

Q <= D;

end

specify

(D => Q) = (1.0, 1.0);

(CLK => Q) = (1.0, 1.0);

(CLRB => Q) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| DFFQX1 | 27.0 | 45.6 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQX1 |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQX1 |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQX1 |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQX1 |  |  |

**Logic Symbol:**

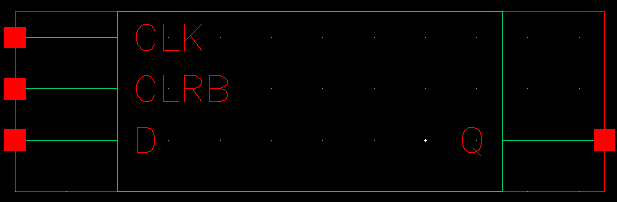
****

Figure 1: Symbol View for the DFFQ cell.

**CMOS Schematic:**

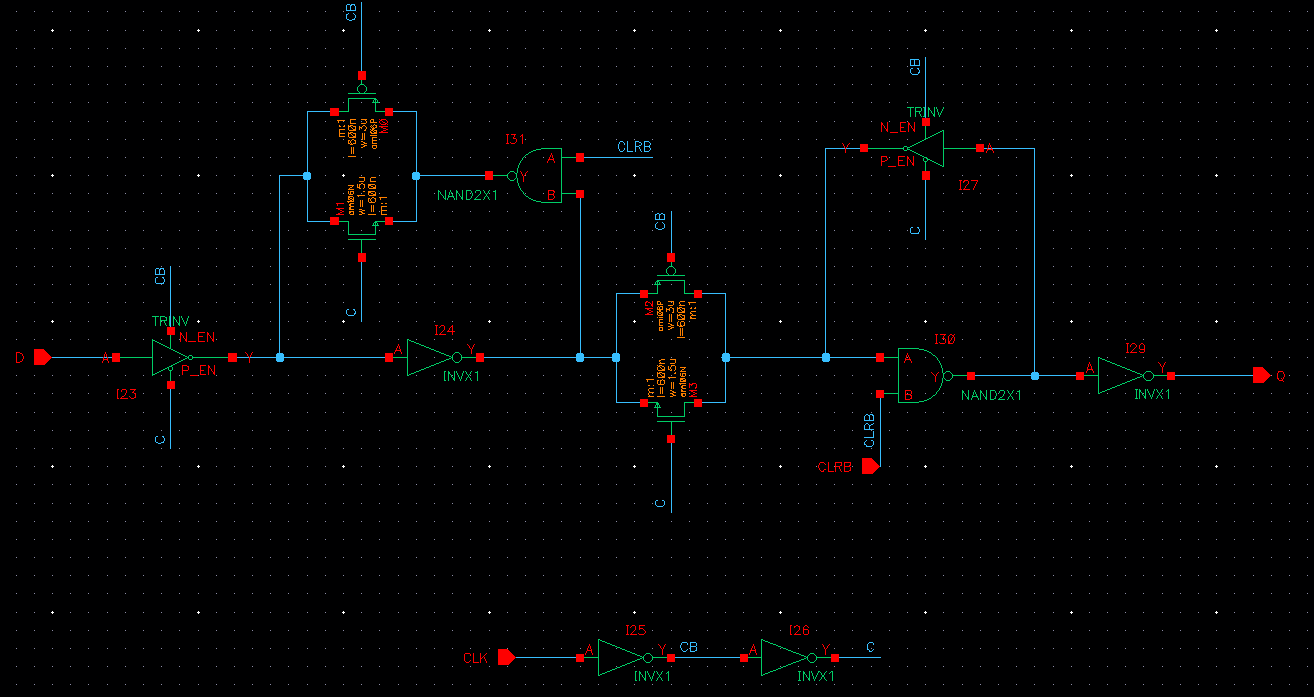
****

Figure 2: CMOS schematic for the DFFQX1 Cell

**CMOS Layout:**

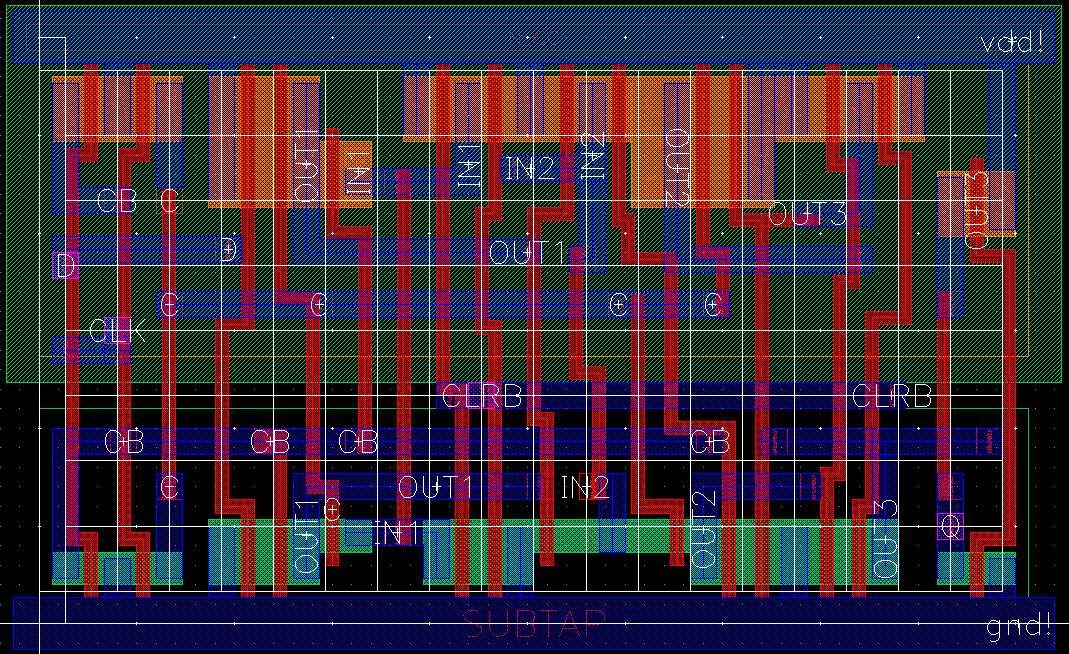
****

Figure 3: CMOS layout for the DFFQX1 cell.